ABSTRACT OF THE DISCLOSURE

When an event takes place in a standby mode, data corresponding to the event is set to a shadow register. The shadow register is operated with a low speed local clock. The contents of the shadow register are copied to a bus IF register through a selector. The bus IF register is connected to a main circuit through a system LSI bus. Data is read from/written to the bus IF register in synchronization with a high speed clock. When the status of the bus IF register changes, a CPU is notified of an interrupt. In a normal mode, an event corresponding to a status change is set to the data bus IF register not through the shadow register. In the standby mode, power of the main circuit is turned off. The high speed clock for the bus IF register is stopped. Thus, the power consumption can be reduced.